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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,765	09/10/2003	Yukiya Hirabayashi	116801	4078

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EXAMINER	
SCHECHTER, ANDREW M	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,765	HIRABAYASHI, YUKIYA	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 March 2006 has been entered.

Response to Arguments

2. Applicant's arguments filed 8 March 2006 have been fully considered but they are not persuasive.

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection. The applicant has amended claims 1 and 6 to recite that the light shielding film has a substantially rectangular frame shape with only a single central opening that encompasses the pixel electrodes in plan view. This distinguishes claims 1 and 6 from the previous prior art, namely *Shirahashi*, in which the light shielding film is formed [see Fig. 15] and has a substantially rectangular frame shape (around the edge of the display), but has multiple central openings which encompass the pixel electrodes in plan view (one opening for each pixel electrode). The amended claims therefore rule out devices in which the light shielding film acts as both a peripheral light shielding

frame and as the black matrix shielding the non-display areas of the individual pixels. The previous rejections of claims 1 and 6 in view of *Shirahashi* are therefore withdrawn.

The applicant argues [pp. 9-10] that *Dill* is unclear on where its sample hold circuit is placed; this is irrelevant. *Dill* is only cited to evidence that it would have been obvious to one of ordinary skill in the art at the time of the invention for a peripheral driving circuit to have a sample hold circuit; other references are relied upon for the location of the peripheral driving circuitry.

Comment on Applicant's Summary of Interview

3. The applicant's "Summary of Substance of Interview" filed on 21 April 2006 states [paragraph bridging pages 1 and 2] that the examiner indicated belief that each of the claim features (as amended) could be found in the prior art, "thereby rendering obvious to one of ordinary skill in the art at the time of the invention the subject matter of the claims". This is not an accurate representation of the examiner's statements or of the examiner's position, which may have been misunderstood by the applicant's representative. Rather, the examiner stated to the applicant's representative that he believed each of the claim features could be found in the prior art, along with reasons why those features were used in the prior art, hence providing motivations for potential rejections under 35 USC 103. The examiner never argued that the mere presence of the features in various prior art references was sufficient to render obvious claims having a combination of those features.

The examiner notes that the applicant's representative did strongly argue that even were the features found, "their specific configuration to meet a specific objective" might not be obvious. In general, of course, this is possible, and depends on the particular limitations, references, and teachings at issue. In the present case, the following obviousness-type rejections are appropriate.

Claim Objections

4. Claim 6 is objected to because of the following informalities: "pixel electrode" in line 9 should be "pixel electrodes". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Murade,* U.S. Patent No. 6,433,841, in view of *Dill et al.,* U.S. Patent No. 3,862,360, and further in view of *Kimura,* Japanese Patent Document No. 11-101985.

Murade discloses an electro-optical device comprising an active matrix substrate [10] having on the same plane a plurality of scanning lines [3a], a plurality of signal lines [6a] provided to intersect the scanning lines, a plurality of pixel electrodes [9a] provided at the intersection portions of the scanning and signal lines, a peripheral driving circuit

[101, 103, 104, etc.] to matrix drive the pixel electrodes, and wiring lines [105a, etc.] for supplying signals to the peripheral driving circuit, the peripheral driving circuit including a sampling circuit [103] with thin film transistors [col. 20, lines 58-60] each having a channel region [a channel region is an inherent part of a TFT]; a counter substrate [20] having a common electrode [21] facing the pixel electrodes; a light shielding film [53] having a substantially rectangular frame shape with only a single central opening that encompasses the pixel electrodes in plan view [see Figs. 5, 6, and 12]; a seal [52] that forms a sealed region between the substrates; a liquid crystal layer [50] disposed in the sealed region between the active matrix substrate and the counter substrate.

Murade discloses a data line "sampling circuit" and various other parts of peripheral driving circuits, but does not use the term "sample hold circuit". First, it appears to the examiner that *Murade's* structure has a sample hold circuit (in that the video data stream is "sampled", and the info is supplied to the data lines and "held" until the next set of data is sampled); the examiner requests the applicant to state explicitly in the response whether they believe that this structure includes a sample hold circuit or not; if so, which part shown constitutes the sample hold circuit, and if not, what is the difference between the disclosed circuit of *Murade* and the recited circuit. (This will hopefully minimize further confusion in the discussion of *Murade* and the "sample hold circuit" limitation".) Second, *Dill* discloses [see Fig. 8-10] an analogous peripheral driving circuit which explicitly includes a sample hold circuit (with TFTs, etc.). It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a sample hold circuit in the device of *Murade*, motivated by the teaching of *Dill* that

this enables a line of conventional video data to be sampled and displayed on the screen [col. 5, lines 15ff.].

Murade does not disclose that the sample hold circuit of the peripheral driving circuit is disposed completely within the sealed region and in a non-overlapping condition with the seal, while the wiring lines for supplying signals to the peripheral driving circuit are disposed at least partially within the seal. *Kimura* discloses [see Figs. 1 and 2, and compare with Figs. 3 and 4] an analogous LCD, in which the analogous peripheral driving circuit is disposed completely within the sealed region and in a non-overlapping condition with the seal, while the wiring lines for supplying signals to the peripheral driving circuit are disposed at least partially within the seal. *Kimura* teaches that this is beneficial because it reduces the amount of wiring passing through the seal, decreasing the level difference on the substrate, and thereby prevents impurities reaching the viewing area and degrading the display [see paragraph 0024, for instance]. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the sample hold circuit of the peripheral driving circuit is disposed completely within the sealed region and in a non-overlapping condition with the seal, while the wiring lines for supplying signals to the peripheral driving circuit are disposed at least partially within the seal in the device of *Murade*, motivated by this teaching of *Kimura*.

Murade does not disclose that both the common electrode and the light shielding film are in a non-overlapping arrangement with both the peripheral driving circuit and the wiring lines in plan view. In addition to its teaching above, *Kimura* also discloses that the peripheral driving circuits are not overlapped by any conductive layers [see Fig. 2

and compare with Fig. 4]. *Kimura* teaches that other conductive films should not be overlapped with the driver circuit, as this can cause the driver to malfunction [see paragraph 0010, for instance]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to have both the common electrode and the light shielding film (both conductive films in *Murade*) in a non-overlapping arrangement with both the peripheral driving circuit and the wiring lines in plan view, as in the arrangement disclosed by *Kimura*, motivated by this teaching of *Kimura*.

Claim 1 is therefore unpatentable.

This combination, as discussed above, meets all the recited limitations of claim 2, so it is also unpatentable.

The peripheral driving circuit comprises at least one of a data line driving circuit [114] and a sample hold circuit [as discussed above], and the wiring lines [to both the data and scanning line driving circuits] comprise at least one of clock signal lines, image signal selecting lines, and image signal lines, so claim 5 is also unpatentable. It is an electronic apparatus, so claim 7 is also unpatentable.

7. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Murade,* U.S. Patent No. 6,433,841, in view of *Dill et al.,* U.S. Patent No. 3,862,360, in view of *Kimura,* Japanese Patent Document No. 11-101985 as applied above, and further in view of *Yamamoto et al.,* U.S. Patent No. 5,506,705.

Murade does not disclose single crystal silicon TFTs or driving signals to the peripheral driving circuit at a frequency equal to or more than 10 MHz. For an analogous LCD, *Yamamoto* discloses using single crystal silicon TFTs and a driving

signal of 10 MHz [col. 12, lines 1-25]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use single crystal silicon TFTs and a 10 MHz driving frequency in the device of *Murade*, motivated by *Yamamoto's* teaching that this allows high speed driving and thus improves the display quality. Claims 3 and 4 are therefore unpatentable.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Murade,* U.S. Patent No. 6,433,841, in view of *Dill et al.,* U.S. Patent No. 3,862,360, in view of *Kimura,* Japanese Patent Document No. 11-101985 as applied above, and further in view of official notice.

The combination discussed above also discloses a method of manufacturing this electro-optical device, including bonding the substrates with a predetermined gap using a sealing material to form a sealed region, and forming a liquid crystal layer in the sealed region. It does not explicitly disclose forming the liquid crystal layer by injecting the liquid crystal into the sealed region. The examiner takes official notice that this is well-known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the injection method for filling the cell with liquid crystal, motivated by its reliability (the technique is conventional and is therefore well-practiced and reliable) and the desire to avoid possible problems involving over- or under-filling the cell which occur when using other methods.

Claim 6 is therefore unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Nelms can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Primary Examiner
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11 June 2006